Remarks and Arguments

The examiner requested that the reference to the U.S. Patent Application on page 7, line 14, of the specification be updated to reflect the current application status. This amendment has been made to indicate that the application is now a U.S. Patent.

Claims 1-9 and 10-19 were rejected under 35 U.S.C. §112, second paragraph, as failing to recite necessary structural relationships between the recited elements. Claims 1-9 and 10-19 have been amended to more particularly specify the structural relationships between the recited components.

For example, claim 1 now recites a port-A interface that receives address signals and data signals from the first multimaster bus, buffers the received address signals and data signals and retransmits data signals received from the second multimaster bus to the first multimaster bus, a port-B interface that retransmits address signals and data signals to the second multimaster bus and receives data signals from the second multimaster bus; and a controller that responds to an address and data received in the port-A interface from the first multimaster bus by controlling the port-B interface to selectively retransmit on the second multimaster bus the received address and data depending on the address bitmap value associated with the received address. Amended claim 1 now clearly recites structural connections between the recited elements.

In addition, claim 10 has been amended to recite first and second unidirectional bus bridges, each of which has a first port-A interface that receives address and data signals from the first multimaster bus, a first port-B interface that is selectively responsive to address and data signals received on the first port-A interface in order to retransmit the address and data signals to the second multimaster bus; and a first controller that selectively passes an address and data received on the first port-A interface from the first multimaster bus to the first port-B interface for retransmission on the second multimaster bus depending on a first address bitmap value associated with the address received on the first port-A interface. Amended claim 10 thus also recites clear structural connections between the recited elements.

Several of the dependent claims have also been amended to clarify relationships between the recited elements. For example amended claim 6 recites the command

interpreter recited in claim 2 comprises another mechanism that transmits a command received from the first multimaster bus on the second multimaster bus when the bridge ID in the received command is in the range of bridge IDs.

Similarly, amended claim 11 recites that each of the first and second unidirectional bridge devices comprises a mechanism for designating whether that unidirectional bridge device will have priority when both the first and second unidirectional bridge devices simultaneously begin a transaction. Amended claim 12 also recites that each of the first and second unidirectional bridge devices further comprises a deadlock mechanism that cooperates with the designating mechanism and the deadlock mechanism of the other unidirectional bridge device for enabling one of the first and second unidirectional bridge devices and disabling the other unidirectional bridge device when both unidirectional bridge devices simultaneously begin a transaction.

Claims 12-19 have also been amended to clarify the claims and correct antecedent bases. For example, new claim 39 has been added to clarify the antecedents in claim 18.

Claims 1-3, 7, 20-22 and 26 have been rejected under 36 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,092,138 (Schutte.) The examiner comments that Schutte discloses the invention as claimed.

The present invention relates to an I^2C bus bridge that can be used to partition a large I^2C bus into smaller bus segments. By programming address bitmaps that are internal to each bridge, the various bus segments can be made to appear as one logical bus. In addition, the bus topology can be designed to maximize the ability to isolate faults within a given segment, thereby improving the ability of technicians to diagnose problems in very large I^2C implementations. In particular, the bus bridges are designed to buffer address and data signals incoming from one bus segment and then selectively retransmit these signals on another bus segment. This retransmission makes it much easier to meet the rise-time specification of the I^2C protocol because the total capacitance of the bus can be reduced by dividing the bus into segments that are not directly connected.

The Schutte reference is also concerned with the capacitance problem but solves the problem in a very different manner. In particular, in order to provide a high speed message transfer mode, Schutte uses a special load circuit that supplies additional current to the bus allowing the load resistor to more quickly pull the bus to the quiescent level. However, since not all I^2C devices can operate in this special high speed mode, a bridge circuit is used to connect a high speed bus segment to a non- high speed bus segment. The bridge circuit either connects the two bus segments together when both segments are operating in normal speed mode or disconnects the segments when one segment is operating in high speed mode. Since the Schutte circuit does not buffer and then retransmit address and data signals it does not provide the isolation and address replication of the present invention. Consequently, when operating in the normal mode, the Schutte system still has the capacitance loading problem.

The claims recite elements not disclosed in the Schutte reference. For example, amended claim 1 recites a port-A interface that receives address signals and data signals from the first multimaster bus and buffers the received address signals and data signals. Schutte discloses no elements in its bridge circuit that buffer address and data signals. Amended claim 1 also recites a port-B interface that retransmits address signals and data signals to the second multimaster bus. The Schutte bus bridge does not retransmit signals. Finally, amended claim 1 recites a controller that responds to an address and data received in the port-A interface from the first multimaster bus by controlling the port-B interface to selectively retransmit on the second multimaster bus the received address and data depending on the address bitmap value associated with the received address. As discussed above, there is no controller in the Schutte bus bridge that causes a retransmission of signals. Instead the controller in the Schutte bus bridge merely connects bus segments together or isolates the bus segments.

Claims 2, 3 and 7 are dependent, either directly or indirectly on amended claim 1 and incorporate the limitations thereof. Therefore, they distinguish over the cited reference in the same manner as amended claim 1.

Claim 20, which is a method claim with limitations paralleling those in amended claim 1, has also been amended in the same manner as claim 1. For example, amended claim 20 now recites the steps of (a) connecting the first multimaster bus to

the second multimaster bus with a bridge having a port-A interface that receives address signals and data signals from the first multimaster bus, buffers the received address signals and data signals and a port-B interface that retransmits address signals and data signals to the second multimaster bus. Claim 20 further recites (b) in response to an address and data received in the port-A interface from the first multimaster bus controlling the port-B interface to selectively retransmit on the second multimaster bus the received address and data depending on the address bitmap value associated with the received address. As discussed above, the Schutte reference does not disclose these steps.

Claims 21, 22 and 26 are dependent, either directly or indirectly on amended claim 20 and incorporate the limitations thereof. Therefore, they distinguish over the cited reference in the same manner as amended claim 20.

Claims 1-9 and 20-28 have also been rejected under 35 U.S.C. §103(a) as obvious over U.S. Patent No. 6,591,322 B1 (Ervin.) Applicant hereby respectfully traverses this rejection. The Ervin reference issued after the filing date of the present application and is therefore a reference solely under 35 U.S.C. §102(e). The invention of this application 09/866,899 and the subject matter of U.S. Patent No 6,591,322 B1 were, at the time the invention of this application 09/866,899 was made, owned by Sun Microsystems, Inc. Consequently, the subject matter of U.S. Patent No 6,591,322 B1 cannot preclude patentability under 35 U.S.C. §103(a) by virtue of 35 U.S.C. §103(c).

Based on the above discussion, claims 1-39 are allowable and advancement of this application to issue is respectfully requested. The Commissioner is hereby authorized to charge any fees or credits under 37 C.F.R. §1.16 and 1.17 to our deposit account No. 02-3038.

Respectfully submitted

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